REMARKS

Claims 1 to 3 and 10 to 13 were pending in the present application. Applicant has amended claims 1 and 11. Claims 1 to 3 and 10 to 13 remain pending.

Claims 1 to 3 and 10, 12, and 13

The Examiner rejected claims 1 to 3, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,049,889 ("Steely, Jr. et al.") in view of U.S. Patent No. 5,850,556 ("Grivna"), and further in view of U.S. Patent No. 5,887,134 ("Ebrahim"). The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over the combination of Steely, Jr. et al., Grivna, and Ebrahim as applied to claim 12, and further in view of U.S. Patent No. 6,038,677 ("Lawlor et al.").

Claim 1

Addressing Applicant's argument that Steely et al. does not disclose a memory copy write command for copying an entire line of memory from a local node to a corresponding line of memory at a remote node, the Examiner stated that Steely et al. discloses a reflective memory where a write to certain memory address space at a local node is reflected to a remote node. January 8, 2009 Office Action, p. 3. Applicant respectfully traverses.

While Steely et al. provides a system that reflects a write to a local node to a remote node, it does not provide a system that accepts a memory copy write command. More specifically, Steely et al. provides the local node with a memory address space that is divided into a local portion and a shared portion, where writes to the shared address space is automatically reflected to the remote node. Steely et al. does not provide the system to accept a memory copy write command.

Addressing Applicant's argument that Steely et al. does not disclose copying an entire line of memory from a local node to a remote node via one of the communication links even when the new data is smaller than the line of memory at the local node, the Examiner stated again that Steely et al. discloses the connection granularity between the nodes is at the page level and therefore an entire 8k byte page at a node is mirrored to another node when less than the entire page is written. January 8, 2009 Office Action, pp. 3 and 4. Applicant respectfully traverses.

Steely et al. does not disclose or suggest that an entire page at a node is mirrored to another node when less than the entire page is written. Steely et al. only discloses that the shared memory space at a node is divided into pages and each page is assigned ("connected") to one or more nodes in the system.

> Thus, connection granularity between nodes in the network is at the page level. Certain nodes in the network will receive data when the CPU writes to one of the N pages of MC address space. The determination of which nodes are mapped to which network addresses, i.e. the mapped connection, are determined at some point prior to when the nodes require data transfer.

Steely et al. col. 4, lines 56 to 64 (emphasis added). The connection granularity simply refers to the correspondence between pages and nodes. For example, Fig. 5 illustrates an example write of 32 byte of data across a data link 20 from node 1 to node 2.

> For example, referring now to FIG. 5, an example write of 32B across the data link 20 from Node 1 to node 2 is shown to include the following steps. First, at step 60, the CPU 22 performs a sequence of 4 Store Quad instructions to an aligned 32 byte address in PCI address space, where each Store Quad instruction has the effect of storing 8 bytes of information. At step 62, the 4, 8 byte stores are converted by the CPU 22 into one aligned 32 byte store command. At step 64, the I/O interface 28 translates the 32 byte store command into a 32-byte PCI write to the corresponding MC address portion of PCI memory space. At step 66, the PCI to MC adapter 34 checks the address of the write command to see if it is to MC address space. If it is, at step 68 the PCI to MC adapter 34 accepts the write, converts it into a 32 byte MC write to the corresponding network address and transmits the request over the data link 20. To convert a PCI address to an MC address, bits <31:27> of the original address are replaced with the contents of the MC base address register 53. The address is then extended to a full 40 bits by assigning zeros to bits <39:32>. At step 70, the PCI-MC adapter at the receiving node accepts the MC write and converts it to a 32 byte PCI write to the corresponding MC page. At step 72, the I/O interface at the receiving node accepts the write and converts it to a 32 byte write to local memory space with an address defined by a corresponding DMA scatter/gather map 57 (FIG. 4).

Steely Jr. et al., col. 5, line 63 to col. 6, line 21. As described above, only 32 byte of data is written at node 1 and only 32 byte of data, and not an entire 8k byte page, is mirrored to node 2. For the reasons above, claim 1 is patentable over the cited references.

Claims 2 to 3 and 10, 12, and 13

Claims 2, 3, 10, 12, and 13 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1. Furthermore, claim 12 is further patentable over the cited references for the following reasons.

The Examiner cited Steely Jr. et al., col. 4, lines 54 to 57 and col. 7, lines 13 to 15, for teaching the details of the memory copy write command as recited in claim 12, in which the existing data is necessarily read, new data merged in a page, and then written and transferred in a reflected memory write to a remote node. January 8, 2009 Office Action, p. 8. Applicant respectfully traverses.

Even assuming an entire page is reflected to a remote node when less than the entire node is written, which the Applicant does not concede, the actions cited by claim 12 are not inherent in such a reflected memory write. For example, the new data may be written into the page, the entire page may be read, and the entire page may be transferred to the remote node. Thus, the recited actions of claim 12 are not inherently disclosed by Steely Jr. et al. For the reasons above, claim 12 is patentable over the cited references.

Claim 11

Claim 11 depends from claim 1 and is patentable over the cited references for at least the same reasons as claim 1. Furthermore, claim 1 is further patentable over the cited references for the following reasons.

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Steely et al., Grivna, and Ebrahim, and further in view of U.S. Patent No. 5,914,970 ("Gunsaulus et al."). Addressing Applicant's argument that the combination of Steely et al., Grivna, Ebrahim, and Gunsaulus et al. does not disclose a DMA write command that causes the computing of a parity over multiple blocks of data from a local memory of the local node and the writing of the parity to a remote memory of the remote node in a single operation, the Examiner stated that a single operation may involve multiple commands. January 8, 2009 Office Action, p. 3. Applicant respectfully traverses.

Claim 11 does not recite multiple commands. Claim 11 recites a single DMA write command that causes both the computing of the parity and the writing of the parity. To further clarify this

point, Applicant has amended claim 11 to recite that the computing of the parity and the writing of the parity are in response to a single DMA write command. For the reasons above, claim 11 is patentable over the cited references.

Summary

In summary, claims 1 to 3 and 10 to 13 were pending in the present application. Applicant has amended claims 1 and 11. Applicant requests the Examiner to withdraw his claim objection/rejections and allow claims 1 to 3 and 10 to 13. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

I hereby certify that this correspondence is being mailed transmitted prior to expiration of the set period of time by being transmitted via the Office electronic filing system in accordance with § 1.6(a) (4).

/David C Hsia/ July 8, 2009
Signature Date

Respectfully submitted,

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